

A15 2 an antifuse address latch coupled to (the address terminals) for latching an antifuse address applied to (the address terminals) corresponding to (the programmable element) to be programmed by the programming event;

logic circuitry coupled to (the address latch) and the data terminals, the logic circuitry receiving (antifuse bank and antifuse address load commands) applied to the data terminals and providing control signals to the antifuse bank address latch and antifuse address latch in response to receiving (the antifuse bank and antifuse address load commands) to cause the antifuse bank address latch and the antifuse address latch to latch (the respective addresses) applied to the external address terminals as (the antifuse bank and antifuse address) corresponding to the programmable element to be programmed, all respectively; and

programming circuitry coupled to the antifuse bank address latch and antifuse address latch and at least a portion of (the programmable elements), the programming circuitry performing the programming event to program (the programmable element) corresponding to (the latched antifuse bank and antifuse addresses.)

A16 32. (Once amended) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

external address terminals;

data terminals;

an array of memory with redundant memory to replace memory cells

9 therein in accordance with (programmed programmable elements);

10 an antifuse bank address latch coupled to (the address terminals) for

11 latching (an antifuse bank address) applied to (the address terminals) corresponding to a bank of

12 antifuses including (a programmable element) to be programmed by a programming event;

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an antifuse address latch coupled to (the address terminals) for latching an

antifuse address applied to (the address terminals) corresponding to (the programmable element) to be programmed by the programming event;

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logic circuitry coupled to (the address latch) and (the data terminals) the

logic circuitry receiving (antifuse bank and antifuse address load commands) applied to the data terminals and providing control signals to the antifuse bank address latch and antifuse address

latch in response to receiving (the antifuse bank and antifuse address load commands) to cause the

antifuse bank address latch and the antifuse address latch to latch (the respective addresses)

applied to the external address terminals as (the antifuse bank and antifuse address) corresponding

to (the programmable element) to be programmed, all respectively; and

programming circuitry coupled to the antifuse bank address latch and

antifuse address latch and at least a portion of (the programmable elements) the programming

circuitry performing the programming event to program (the programmable element)

corresponding to the latched antifuse bank and antifuse addresses.

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